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| 09/152,266 | 09/14/1998 | ERIC R. CAMPBELL | 540-127 | 8971 |

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| EXAMINER | |
|---|---|
| PHAM, THOMAS K | |

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|---|---|
| 2121 | 13 |

DATE MAILED: 02/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/152,266 | CAMPBELL ET AL. | |
| | Examiner | Art Unit | |
| | Thomas K Pham | 2121 | |

*-- The MAILING DATE of this communication app ars on the cover she t with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *2-19 and 22-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-19 and 22-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

### *Response to Amendment*

1. This action is in response to request for re-consideration filed on 12/02/2003.

2. New claims 22-41 filed by the applicant have been entered.

3. The indicated allowability of claims 2 and 10 are withdrawn in view of the newly discovered reference(s) to Breuninger European Patent No. 0 266 065. Rejections based on the newly cited reference(s) follow.

## DETAILED ACTION

### *Claim Objections*

4. Claims 17, 38 and 39 are objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to further limit the subject matter of a previous claim. Applicant is required to cancel the claim(s), or amend the claim(s) to place the claim(s) in proper dependent form, or rewrite the claim(s) in independent form. "A processing network" is not further limit the subject matter of a previous claim.

### *Claim Rejections - 35 USC § 103*

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 2-20 and 22-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennings et al. U.S. Patent No. 4,796,178 (hereinafter Jennings) in view of Breuninger European Patent No. 0 266 065.

**Regarding claim 2**

Jennings teaches an integrated circuit for use as a scheduler of activities to be run on an associated processor (col. 3 lines 27-24, "The system includes a ... by way of controller 12a") but does not teach the modular structure and constructed from an assembly of tiles, wherein each tile defines a building block having logic and structure, said tiles being abutted one against the other to form a two-dimensional array of n rows and m columns which realizes an overall functionality for the integrated circuit and wherein each of the 'n' rows of tiles provides the control logic for each one of 'n' schedulable activities and each of the m columns of tiles provides a particular function. However, Breuninger teaches the programmable sequence generator that has a plurality of field-programmable elements, including AND and OR matrix representing two dimensional logic gates (page 3 lines 28-40, "a simplified electrical diagram of ... line are blown open"). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the programmable sequence generator of Breuninger with the integrated circuit of Jennings because it would provide for to output a plurality of clock sequences to aid in the computation how long a particular process in a wait state in order to compute process priorities of the scheduling tasks.

**Regarding claim 3**

Breuninger teaches a further row of tiles for interfacing with an associated central processor and for generating control signals for said two-dimensional array (page 5 lines 14-26, "A RESET line 98 connects processor 90 ... is to be accessed").

**Regarding claim 4**

Jennings teaches the control logic includes means for holding control variables corresponding to each of said activities and next-activity selection logic for identifying those activities which are ready for running on the processor, depending on the status of said control variables (col. 4 lines 32-54, "the task control processor 13 ... had the highest priority").

**Regarding claim 6**

Jennings teaches setting those control variables comprising a "stim-wait" channel in response to a signal received from an associated processor (col. 7 lines 51-57, "The SIMPLE-WAIT command ... a set events has happened").

**Regarding claim 7**

Jennings teaches setting those control variables comprising a "stim-wait" channel in response to a signal received from an associated peripheral device (col. 3 lines 27-34, "The system includes a plurality of ... by way of controller 12a").

**Regarding claim 8**

Jennings teaches setting those control variables comprising a "stim-wait" channel in response to a signal received from a second integrated circuit as described and claimed herein (col. 8 line 58 to col. 9 line 11, "In WORD-3 of FIG. 4B ... move to this stack number").

**Regarding claims 9 and 30**

Jennings teaches temporarily inhibiting any changes to control variables from entering the next-activity-selection logic (col. 9 lines 8-10, "Bit 2, when set, ... move to this stack number").

**Regarding claim 10**

Breuninger teaches incorporating decoding and encoding logic for routing signals, identifying one or more of said 'n' activities, between the associated central processor and the appropriate row of tiles (page 10 lines 31-44, "These product terms are then ... equations need be written").

**Regarding claim 13**

Jennings teaches detecting when a schedulable activity has a higher priority than that activity currently running on an associated central processor and thereby generating an interrupt signal (col. 11 lines 64-68, "the device requesting the interrupt ... status change to "has occurred" " ).

**Regarding claim 14**

Jennings teaches incorporating a counter circuit (col. 10 lines 41-43, "The selected address ... process RAM 50").

**Regarding claim 15**

Jennings teaches configured for asynchronous operation, by incorporating level-driven, clock-free ripple logic (col. 11 lines 50-61, "FIG. 9B illustrates how ... available processor 10 of FIG. 1").

**Regarding claim 17**

Jennings and Breuninger teach processing network responsive to an activity scheduler as rejected in claim 22.

**Regarding claims 18, 40 and 41**

Jennings teaches at least one peripheral device for setting at least one control-variable in said integrating circuit (col. 3 lines 27-34, "The system includes a plurality of ... by way of controller 12a"). Reference indicated that any of the processors connected to the memory controllers including the I/O processor (peripheral) is capable of performing the task controlling process.

**Regarding claim 19**

Jennings teaches a multiprocessor network comprising a plurality of processors (fig. 1, element 10), each responsive to an activity scheduler, wherein the activity schedulers are linked together (col. 4 lines 32-54, "the task control processor ... had the highest priority").

7. Claims 22-29, 31, 34-35, 38 and 39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennings.

**Regarding claim 22**

Jennings teaches an activity scheduler arranged to control activities in a processor, comprising: an integrated circuit to support data and multi-tasking for the processor (col. 2 lines 24-28, "the basic functions ... of the individual tasks"), the integrated circuit being configured to support a control node mechanism comprising a set of stim-wait channels circuit (col. 3 lines 27-34, "The system includes a plurality of ... by way of controller 12a") but does not teach each stim-wait channel incorporating holding means to hold a pair of control variables for one of said activities, and the integrated circuit further incorporating next activity logic to identify each activity that is ready to run on the processor. However, Jennings teaches the task control processor 13 for handling the scheduling of various tasks by holding control variables in the linked list to process each activity according to the status of various event designations called (col. 4 line 55 to col. 5

line 39, "the task control processor 13 ... liberated by its owning process"). It is obvious to one of ordinary skill in the art that function of the task control processor 13 of Jennings teaches limitations as claimed.

**Regarding claim 23**

Jennings teaches an activity scheduler arranged to control activities in a plurality of processors (fig. 1, elements 10), comprising: a separate integrated circuit to support shared data and multi-tasking for each of said processors (col. 2 lines 24-28, "the basic functions ... of the individual tasks"), each integrated circuit being configured to support a control node mechanism comprising a set of stim-wait channels (col. 3 lines 27-34, "The system includes a plurality of ... by way of controller 12a") but does not teach each stim-wait channel incorporating holding means to hold a pair of control variables for one of said activities, and each of said separate integrated circuits further incorporating next activity logic to identify each activity that is ready to run on the associated processor. However, Jennings teaches the task control processor 13 for handling the scheduling of various tasks by holding control variables in the linked list to process each activity according to the status of various event designations called (col. 4 line 55 to col. 5 line 39, "the task control processor 13 ... liberated by its owning process"). It is obvious to one of ordinary skill in the art that function of the task control processor 13 of Jennings teaches limitations as claimed.

**Regarding claim 24**

Jennings teaches an activity scheduler arranged directly to support shared data and multi-tasking in a network of processors(col. 2 lines 24-28, "the basic functions ... of the individual tasks"), comprising: a separate integrated circuit to support each of said processors (fig. 1, elements 10),

each integrated circuit being configured to control a control node mechanism comprising a set of stim-wait channels (col. 3 lines 27-34, "The system includes a plurality of ... by way of controller 12a") but does not teach each stim-wait channel incorporating holding means to hold a pair of control variables for one of said activities, and each of said separate integrated circuits further incorporating next activity logic to identify each activity that is ready to run on the associated processor. However, Jennings teaches the task control processor 13 for handling the scheduling of various tasks by holding control variables in the linked list to process each activity according to the status of various event designations called (col. 4 line 55 to col. 5 line 39, "the task control processor 13 ... liberated by its owning process"). It is obvious to one of ordinary skill in the art that function of the task control processor 13 of Jennings teaches limitations as claimed.

**Regarding claim 25**

Jennings teaches at least one of said processors is arranged to set at least one control variable in one of said separate integrated circuits (col. 8 line 58 to col. 9 line 11, "In WORD-3 of FIG. 4B ... move to this stack number").

**Regarding claim 26**

Jennings teaches a peripheral device arranged to set at least one control variable in one of said separate integrated circuits (col. 8 line 58 to col. 9 line 11, "In WORD-3 of FIG. 4B ... move to this stack number"). Reference indicated that any of the processors connected to the memory controllers including the I/O processor (peripheral) is capable of performing the task controlling process.

**Regarding claim 27**

Jennings teaches at least one of said separate integrated circuits is arranged to set at least one control variable in another of said separate integrated circuits (col. 8 line 58 to col. 9 line 11, "In WORD-3 of FIG. 4B ... move to this stack number").

**Regarding claim 28**

Jennings teaches at least one control node mechanism has its set of stim-wait channels arranged as an array comprising n rows and m columns, and at least one of said separate integrated circuits is configured to support said array of control node mechanisms (col. 3 lines 27-34, "The system includes a plurality of ... by way of controller 12a").

**Regarding claims 29 and 35**

Breuninger teaches the control variables are Boolean (page 3 lines 28-40, "a simplified electrical diagram of ... line are blown open"). Prior art teaches AND and OR gates matrixes which control variables are Boolean as well known in the art.

**Regarding claim 31**

Jennings teaches incorporating decoding and encoding logic to identify one or more of said activities and to route signals from said activity scheduler to the appropriate stim-wait channel (col. 7 lines 7-15, "The various commands described ... processors executing that process").

**Regarding claim 34**

Jennings teaches a priority detector to detect an activity having a priority higher that the priority of an activity being processed on one of said processors, the priority detector being arranged to generate an interrupt signal to interrupt processing of the lower priority activity in favour of the higher priority activity (col. 11 lines 64-68, "the device requesting the interrupt ... status change to "has occurred" " ).

**Regarding claim 36**

Jennings teaches a method of controlling activities in a processor but does not teach holding a pair of control variables in respect of each activity, identifying the next activity to be run on the processor, and selecting the pair of control variables associated with the said next activity. However, Jennings teaches the task control processor 13 for handling the scheduling of various tasks by holding control variables in the linked list to process each activity according to the status of various event designations called (col. 4 line 55 to col. 5 line 39, "the task control processor 13 ... liberated by its owning process"). It is obvious to one of ordinary skill in the art that function of the task control processor 13 of Jennings teaches limitations as claimed.

**Regarding claim 37**

Jennings teaches a method of controlling activities in a plurality of processors but does not teach holding a pair of control variables in respect of each activity in each processor, identifying the next activity to be run on each processor, and selecting the pairs of control variables associated with the next activity of each processor. However, Jennings teaches the task control processor 13 for handling the scheduling of various tasks by holding control variables in the linked list to process each activity according to the status of various event designations called (col. 4 line 55 to col. 5 line 39, "the task control processor 13 ... liberated by its owning process"). It is obvious to one of ordinary skill in the art that function of the task control processor 13 of Jennings teaches limitations as claimed.

**Regarding claim 38**

Jennings and Breuninger teach a processing network responsive to an activity scheduler as rejected in claim 23 above.

**Regarding claim 39**

39. Jennings and Breuninger teach a processing network responsive to an activity scheduler as rejected in claim 2 above.

8. Claims 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jennings in view of Breuninger and further in view of Bass et al. U.S. Patent No. 5,487,170 (hereinafter Bass).

**Regarding claims 11 and 32**

Jennings and Breuninger teach an integrated circuit in which the next-activity-selection logic includes means for selecting the next activity but does not teach the activity to be run on a round robin basis. However, Bass teaches the activity to be run on a round robin basis (col. 7 lines 19-24, "Select logic made up of ... round robin scheme"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the round robin basis of Bass to the task control mechanism of Jennings and Breuninger because it would provide for assuring that each task will have access to system resources.

**Regarding claims 12 and 33**

Jennings and Breuninger teach an integrated circuit in which the next activity selection logic includes means for allocating differing priority levels to groups of activities, and for selecting the next activity but does not teach the activity to run within a group on a round robin basis within that group. However, Bass shows a data processing system in which the next activity selection logic includes means for allocating differing priority levels to groups of activities, and for selecting the next activity to run within a group on a round robin basis within that group (col. 7

lines 25-37, "select logic 1102 matched ... access to system resources"). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the round robin basis of Bass to the task control mechanism of Jennings and Breuninger because it would provide for assuring that each task will have access to system resources.

**Regarding claim 16**

Jennings and Breuninger teach an integrated circuit but does not teach being fabricated using CMOS techniques. "Official Notice" is taken that both the concept and advantages of fabricated the integrated circuit using CMOS techniques is well known and expected in the art. It would have been obvious to one of ordinary skill in the art to include the fabrication of the integrated circuit using CMOS techniques to the task control mechanism of Jennings and Breuninger because it would provide for low power consumption or essentially zero when the circuit elements are not being clocked or changing level.

***Conclusion***

9. Applicant's submission of an information disclosure statement under 37 CFR 1.97(c) with the fee set forth in 37 CFR 1.17(p) on 11/12/2003 prompted the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 609(B)(2)(i). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner *Thomas Pham*; whose telephone number is (703) 305-7587 and fax number is (703) 746-8874. The examiner can normally be reached on Monday-Thursday and every other Friday from 7:30AM- 5:00PM EST or contact Supervisor, *Mr. Anil Khatri*, can be reached on *(703) 305-0282.*

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

**Thomas Pham**
*Patent Examiner*

TP

February 23, 2004

ANIL KHATRI
SUPERVISORY PATENT EXAMINER